MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

ECP4256 – PRACTICAL FPGA DESIGN AND INTERFACING

(All sections / Groups)

10 MARCH 2016
2:30 p.m – 4:30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 5 pages with 5 Questions only.
2. Attempt **ALL** questions.
3. Please write all your answers in the Answer Booklet provided.

Question 1

i) Discuss the advantages and disadvantages of the following programmable logic technology.

a) SRAM-based [2 marks]

b) Anti-fuse technique [2 marks]

ii) Compare the following **TWO** programmable logics. In your opinion, which programmable logic is better in implementing "Sum-Of-Products" binary logic equation.

a) Programmable Logic Array (PLA) [3 marks]

b) Programmable Array Logic (PAL) [3 marks]

iii) Logic Element (LE) is the smallest unit of a logic in Altera Field Programmable Gate Array (FPGA). With the aid of an LE diagram given below (Figure Q1(iii)), describe any **FIVE** Altera LE features.

[10 marks]

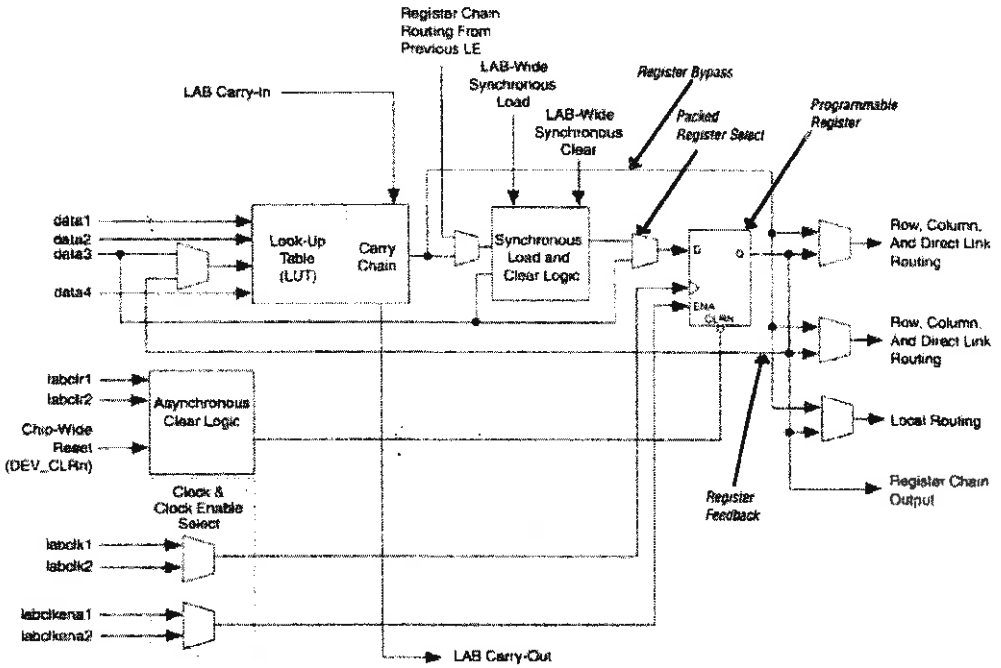

Figure Q1(iii)

Continued.....

Question 2

i) Implement the following digital logic using Verilog HDL (Hardware Description Language).

a) Gate network is as illustrated in Figure Q2(i)(a) [5 marks]

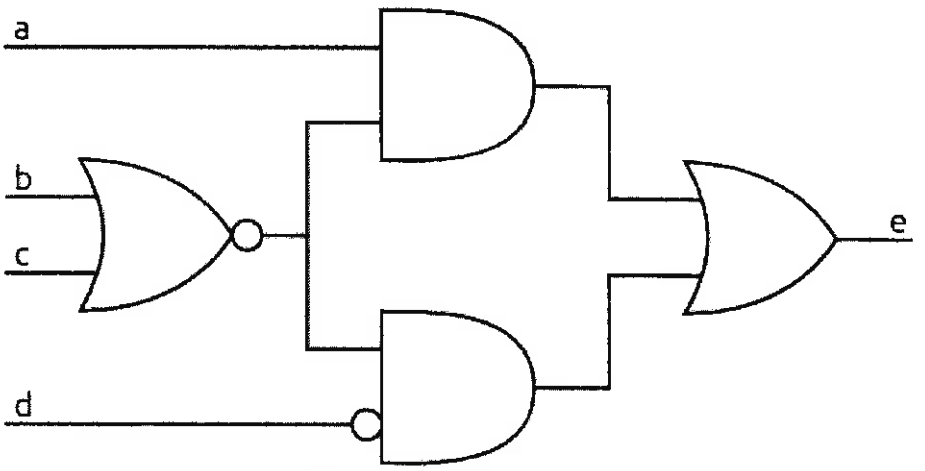

Figure Q2(i)(a)

b) Word size positive edge clocked binary decrementing counter with Synchronous Load. [5 marks]

ii) Write a testbench to verify the functionality of the logic circuit in,

a) Question 2, Part (i) (a) [5 marks]

b) Question 2, Part (i) (b) [5 marks]

Question 3

i) Briefly discuss what process pipelining is. [2 marks]

ii) You are given a task to improve a sequential design of two matrix multiplication for a digital image processor. With the aid of a diagram, explain how the following techniques helps in improving the latency of your design.

a) Loop unrolling [6 marks]

b) Chaining [6 marks]

c) Multi-cycling [6 marks]

Continued.....

Question 4

i) Using the Verilog HDL kick-start code give below, [15 marks]

```
module reverse_controller(
  input clk,
  input reset,
  input [7:0] data,
  output LED_far, LED_mid, LED_near,
  output BUZZER
);

/* Your functionality design codes */


endmodule
```

Design a vehicle reverse sensor controller for Proton Sdn. Bhd. Below are the behavioral descriptions of the vehicle reverse sensor controller.

- A 100 Hz clock source is connected to `clk` pin.
- Distance sensor outputs the following data for the following distance range,
  - Far (`8'b0000_0000 - 8'b0111_1111`)
  - Mid (`8'b1000_0000 - 8'b1111_0000`)
  - Near (`8'b1111_0001 - 8'b1111_1111`)
- Indicator (buzzer & LED) buzz/flash at the following frequencies for the following distance range,
  - Far (1 Hz)
  - Mid (2 Hz)
  - Near (10 Hz)

ii) Write a testbench to verify the functionality of your design. [5 marks]

Continued.....

Question 5

i) Discuss **FIVE** advantages of digital system utilizing System on Programmable Chip (SoPC) over fixed processor. [5 marks]

ii) Altera FPGA supports "Hard" core processor and "Soft" core processor system. Compare "Hard" core processor and "Soft" core processor system. Give an example for each type of the processor system. [4 + 2 marks]

iii) Design an SOPC system on an Altera Cyclone II FPGA chip for a Blue Ray Player with the following features,

- Disc reader with 2 channels of Low Voltage Differential Signalling (LVDS) interface (1 channel for video and 1 channel for audio) & single channel SPI for motor control.
- The video data will be sent to TV through HDMI interface.
- The audio data will be sent to home theatre system through Bluetooth interface.
- Buttons for user input that were connected through parallel input interface.
- LCD display with I^2C interface.

** Use a block diagram to illustrate your system and describe the functionality / purpose of each block.* [9 marks]

End of Paper